Course Number & Name: EEE 4329 / 5400 - Future of microelectronics circuits

(Fall 2014  CLASS on EDGE Lectures on E-Learning)

Credits and Contact Hours: 3 crs; 3 classes per week of 50 minutes each

Instructor’s or Course Coordinator’s Name: Dr. Scott E. Thompson

Instructor  Prof. Scott Thompson  
535 Engineering Bldg  
846-0320  
Office hours: Thurs 8:30 to 10:00  
Tues 8:30 to 10:00  
Plus e-learning discussion board (https://lss.at.ufl.edu/)  
(Plus additional office hours arranged email thompson@ece.ufl.edu)

Grader: (Seahee Hwangbo) Office hrs: Monday 10:40-11:40  hwangbo55@ufl.edu

Textbook Title, Author, and Year: Nanoelectronics and Information Technology 2003 or equivalent. Textbook OPTIONAL

a. Supplemental Material: ~15 journal papers and handouts

Specific Course Information
a. Catalog Description: Analysis and design of possible future transistor technology to fabricate microelectronics circuits
b. Prerequisites or Co-requisites: Electronics I, Solid State Devices, Basic knowledge of semiconductor physics and devices. The class will be introductory and targeted towards students with a diverse background from electronics to material science. The class will be designed to introduce CMOS, non classical CMOS, and post CMOS device concepts without a quantum mechanical background.

c. Required, Elective, or Selected Elective (Table 5-1):

Specific Goals for the Course
a. Specific Outcomes of Instruction:  
This course focuses on analysis and design transistors for the fabrication of future microelectronic circuits and memory. A very brief introduced and described CMOS digital and memory technology will be introduced along with Moore's law and scaling trends. Next class will most of the time on analysis of potential technologies to replace Si CMOS transistors.

b. Explicitly indicate which of the student outcomes listed in Criterion 3 or any other outcomes are addressed by this course:  
EE2, a, c, e, I, k
Brief List of Topics to Be Covered

- Moore’s Law and microelectronic industry trends
  - History of Computing / Anatomy of an Ipad
  - Chip technology / nonmanufacturing in Ipad (Logic chips, RF analog, DRAM, NAND, CMOS image sensor, motion sensors)

- State of the art: logic technology
  - 20nm /16m, 14nm, 10nm, planar and FinFET.
    - Design rules/ double and triple patterning /SRAM layout

- Start of the art: memory devices (DRAM and NAND FLASH)
- Logic and memory technology limits / Nanofabrication limits
  - Lithography
    - 193i, EUV
  - Devices limits: quantum-statistical
- Display technology: current technology and future trends
- Next wave of computing (internet of things / wearable electronics)
  - Near threshold computing?
- Post conventional CMOS, DRAM and NAND technologies
  - gate all around CMOS, III-V material, 3D,
  - Carbon nanotubes transistors
  - Single electron devices for Logic applications
  - Other??

- Grading:
  - 85%
    - 20% Exam 1: Tues Sept 30
    - 20% Exam 2: Tues, Oct 21
    - 20% Exam 3: Tues, Dec 2
    - 25% Comprehensive final exam as scheduled by college

  - No exam make-up unless valid excuse. All valid excuses must be approved by the Professor.

  - 5% Homework
  - 10% Project

  - Final Grading Scale

  - ≥90% → A; ≥86.67% → A-; ≥83.33% → B+; ≥80% → B; ≥76.67% → B-;
    ≥73.33% → C+; ≥70% → C; ≥66.67% → C-; ≥63.33% → D+; ≥60% → D;
    ≥56.67% → D-; <56.67% → E
• Attendance: Due to quantity and research nature of material, it is important to make every attempt to attend class or watch all class lectures. Class attendance is required on days I announce class discussions.